AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1.-2. (canceled)

3. (previously presented): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape-provided along a side wall portion and a bottom portion of a hole provided in an interlayer insulating film and has a thickness of 30 nm or greater at the bottom portion of said lower electrode and a thickness of less than 30 nm at a side wall portion of said lower electrode.

4. - 8. (cancelled):

9. (previously presented): A semiconductor device comprising memory cells each having an MISFET for memory selection formed on a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and a

second metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film,

wherein said lower electrode has a cup shape provided along a side wall portion and a bottom portion of a hole provided in an interlayer insulating film, said first metal layer and said second metal layer partly contact each other, said lower electrode is connected at an entire bottom of said lower electrode to said second metal layer and said lower electrode has a thickness of 30 nm or greater at the bottom portion of said lower electrode and a thickness of less than 30 nm at a side wall portion of said lower electrode.

10 - 52. (cancelled)

53. (Previously Presented): The semiconductor device according to claim 3, wherein said lower electrode is a metal film.

54. (Previously Presented): The semiconductor device according to claim 3, wherein said lower electrode is a ruthenium film.

55. (Previously Presented): The semiconductor device according to claim 3, wherein said capacitive insulating film is a tantalum oxide film.

56. (Previously Presented): The semiconductor device according to claim 3, wherein said upper electrode is a ruthenium film.

57. (Previously Presented): The semiconductor device according to claim 3, wherein said first metal layer is a titanium nitride film.

58. (Previously Presented): The semiconductor device according to claim 9, wherein said lower electrode is a metal film.

59. (Previously Presented): The semiconductor device according to claim 9, wherein said lower electrode is a ruthenium film.

60. (Previously Presented): The semiconductor device according to claim 9, wherein said capacitive insulating film is a tantalum oxide film.

61. (Previously Presented): The semiconductor device according to claim 9, wherein said upper electrode is a ruthenium film.

62. (Previously Presented): The semiconductor device according to claim 9, wherein said first metal layer is a titanium nitride film.